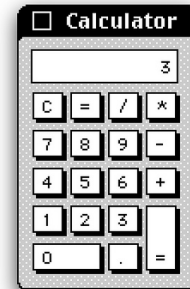


## Digital Logic Projects:

- Complex logic equations to circuits using mixed-logic impletations of Small Scale Integration (SSI) digital circuit chips
- Built a 4-to-1 MUX using SSI chips
- Built a 2-to-4 Decoder using SSI chips
- Built a 4 input priority encoder using SSI chips
- Designed 4-bit Arithmetic Logic Unit (ALU) on an Altera 7064 CPLD
  - two 4-bit inputs
  - two function-select inputs
  - a carry input
  - 4-bit function output
  - performs the following functions:
    - bit-wise OR
    - bit-wise AND
    - sum
    - complement of A
- Designed a 4-bit Counter using D-flip-flops on a CPLD
  - Hardware switch debouncing
  - Forward/reverse select
  - Asynchronous set and clear
  - Output flag when any desired number is reached
- Designed a traffic light controller using CPLD
  - Designed and implemented using an algorithmic state machine (ASM)
  - Hardware switch debouncing
  - Sensor dependent
  - D, T, and JK flip-flops
- Designed an Elementary CPU on a CPLD
  - 3-bit instruction field to control ASM
  - program counter
  - memory module to store programs
  - two 4-bit registers
  - Bus select for ALU with MUXs
  - Instructions:
    - Move register A to register B
    - Load register A with data on the input bus
    - Left shift register A 1 bit, put back into A
    - Sum register A and register B, put into A
    - Load PC with input bus
    - Shift register A right one bit



## Digital Design Projects. All projects in VHDL on an Altera Cyclone II FPGA

- SSI Designs
  - 8-bit counter
  - 1-bit full-adder
  - 4-bit ripple-carry
- MSI combinatorial circuits
  - 4-to-1 MUX



- 3-to-8 decoder
- 7-segment LED decoder
- 8-bit adder
- 8-bit adder to 7-segment decoder
- 16-to-4 MUX
- 8-bit look-ahead carry adder (LCA)
  - Controlled with dip-switches
  - Connected to 7-segment LEDs
  - Hierarchical circuit design
  - Composed of:
    - 2-bit LCA generators
    - 4-bit LCA adders
- 8-bit ALU
  - Hierarchical design
  - Integrated with push buttons and 7-segment LEDs
  - Functions:
    - Zero
    - Add with carry
    - Subtract using two's complement
    - Shift right
    - Shift left
    - Bit-wise XOR
    - Bit-wise AND
    - Bit-wise OR
- VGA image generator
  - Reads MIF files and generates the appropriate signals to display on a VGA monitor.
- Design and implementation of a 32-bit FIR Filter
  - Algorithmic state machine used to control a data path component with parallelism through functional decomposition/replication and pipelining.
- Designed a simple computer
  - 8-bit processor
  - 64K address space
  - RAM
  - I/O ports



### Microprocessors. Using a TI C2000 DSP

- Assembly program to sort 2's complement 16-bit numbers in order of magnitude
- 16-button keypad scanning program, using 8 i/o lines
- Software switch debouncing
- Interfacing with external output and input ports connected directly to data bus
- Interfacing with external SRAM connected directly to the address and data busses
- 16x2 LCD display driver
- A real-time stopwatch using timer interrupts



- Start/stop button
  - Reset button
- Program to write and read ascii characters to and from a computer
  - Read data displayed on LCD
  - Controlled using built-in Serial Communication Interface (SCI) FTDI USB Controller
  - Written in both assembly and C++
- A simple multimeter to measure 0 to 3.3 Volts with 0.1 V accuracy
- Wavetable audio signal generator
  - Plays any 64 sample wave put into the wavetable from 100 to 1000 Hz, both a coarse frequency potentiometer and 16 discrete frequencies

